//testbench

module threebcomtb;

reg [2:0] a,b;

wire p, q, r;

threebcom uut( .a(a), .b(b), .p(p), .q(q), .r(r));

initial begin

$dumpfile("threebcom.vcd");

$dumpvars(1);

end

initial begin

a = 4'b0011; b = 4'b0000;

#10;

a = 4'b0000; b = 4'b0001;

#10;

a = 4'b1000; b = 4'b1000;

#10;

$finish;

end

endmodule

// design

module threebcom(a, b, p, q, r);

input [2:0] a,b;

output p, q, r;

assign p = (a == b);

assign q = (a > b);

assign r = (a < b);

endmodule